Electronic Version
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Claims

[c1] 1. A chip package structure, comprising:
a carrier;
a chip, having an active surface with a plurality of bumps thereon, wherein the chip is flipped over and bonded to the carrier in a flip-chip bonding process so that the chip and the carrier are electrically connected;
a heat sink, set over the chip; and
an encapsulating material layer, filling a bonding gap between the chip and the carrier as well as a gap between the heat sink and the chip, wherein the encapsulating material layer is formed in a simultaneous molding process and part of the surface of the heat sink away from the chip is exposed.

[c2] 2. The chip package structure of claim 1, wherein the chip is separated from the heat sink by a distance between 0.03 ~ 0.2mm.

[c3] 3. The chip package structure of claim 1, wherein the encapsulating material layer has a thermal conductivity greater than 1.2W/m.K.

[c4] 4. The chip package structure of claim 1, wherein mate-

rial constituting the encapsulating material layer comprises a resin.

[c5] 5. The chip package structure of claim 1, wherein material constituting the heat sink comprises a metal.

[c6] 6. The chip package structure of claim 1, wherein the package further comprises an array of solder balls attached to a surface of the carrier away from the chip.

[c7] 7. The chip package structure of claim 1, wherein the package further comprises at least a passive component set on and electrically connected with the carrier.

[c8] 8. The chip package structure of claim 1, wherein the carrier is selected from a group consisting of a packaging substrate or a lead frame.

[c9] 9. A chip package structure, comprising:
a carrier;
a chipset, set over and electrically connected to the carrier, wherein the chipset comprises a plurality of chips, at least one of the chips is bonded to the carrier or another chip in a flip-chip bonding process so that a flip-chip bonding gap is created;
a heat sink, set over the chipset; and
an encapsulating material layer, filling the flip-chip bonding gap and a gap between the chipset and the heat

sink, wherein the encapsulating material layer is formed in a simultaneous molding process and part of the surface of the heat sink away from the chipset is exposed.

[c10] 10. The chip package structure of claim 9, wherein the chipset is separated from the heat sink by a distance between 0.03 ~ 0.2mm.

[c11] 11. The chip package structure of claim 9, wherein the encapsulating material layer has a thermal conductivity greater than 1.2W/m.K.

[c12] 12. The chip package structure of claim 9, wherein the chipset at least comprises:
a first chip, having a first active surface, wherein the first chip is attached to the carrier such that the first active surface is positioned away from the carrier; and
a second chip, having a second active surface with a plurality of bumps thereon, wherein the second active surface of the second chip is bonded and electrically connected to the first chip in a flip-chip bonding process such that the bumps between the second chip and the first chip set a flip-chip bonding gap.

[c13] 13. The chip package structure of claim 12, wherein the chipset further comprises a plurality of conductive wires with ends connected electrically to the first chip and the

carrier respectively.

[c14] 14. The chip package structure of claim 9, wherein the chipset at least comprises:
a first chip, having an active surface with a plurality of first bumps thereon, wherein the first active surface of the first chip is bonded and electrically connected to the carrier in a flip-chip bonding process such that the first bumps between the first chip and the carrier set a flip-chip bonding gap;
a second chip, having a second active surface, wherein the second chip is attached to the first chip such that the second active surface is positioned away from the first chip; and
a third chip, having a third active surface with a plurality of second bumps thereon, wherein the third active surface of the third chip is bonded and electrically connected to the second chip in a flip-chip bonding process such that the second bumps between the third chip and the second chip set another flip-chip bonding gap.

[c15] 15. The chip package structure of claim 14, wherein the chipset further comprises a plurality of conductive wires with ends electrically connected to the second chip and the carrier respectively.

[c16] 16. The chip package structure of claim 9, wherein the

material constituting the encapsulating material layer comprises a resin.

[c17] 17. The chip package structure of claim 9, wherein the material constituting the heat sink comprises a metal.

[c18] 18. The chip package structure of claim 9, wherein the package further comprises an array of solder balls attached to a surface of the carrier away from the chipset.

[c19] 19. The chip package structure of claim 9, wherein the package further comprises at least a passive component set on and electrically connected with the carrier.

[c20] 20. The chip package structure of claim 9, wherein the carrier is selected from a group consisting of a packaging substrate or a lead frame.